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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,301	06/06/2001	Daniel Schoch	231008-0352	9521

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EXAMINER

HUYNH, KIM T

ART UNIT	PAPER NUMBER
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2189

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DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

924

Office Action Summary	Application No. 09/876,301	Applicant(s) SCHOCH ET AL.	
	Examiner Kim T. Huynh	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 January 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 and 15-24 is/are rejected.
- 7) ☒ Claim(s) 14 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
 a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 7-13, 15-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Massie (Pub. No US 20030023908)

As per claim 1, Massie discloses an electronic device comprising:

- A controller programmed to produce first address data on an output thereof;[0005-0006]
- A plurality of integrated circuits(Ics) addressable by the controller; [0008] and
- A shared bus joining the controller and the plurality of Ics;[0048], [0005]
- Wherein each of the Ics comprises an input for receiving address data representing an address of the IC on the shared bus, and an output for providing incremented address data, and [0048-0051]
- Wherein the input of a first IC communicates with output of the controller and the inputs of succeeding Ics communicate with the outputs of preceding Ics in a daisy chain configuration. [0051-54], [0089, claim 7]

As per claim 2, Massie discloses wherein each of the lcs further comprises a processor programmed to receive address data at the input, store the address data as the address of the IC, increment the address data, and provide the incremented address data at the output.[0051], [0054-0055], [0063]

As per claim 3, Massie discloses wherein each of the lcs further comprises an address register for storing address data received at its input, and output generator logic for incrementing the address data.[0051], [0054-0055]

As per claim 4, Massie discloses wherein each of the lcs further comprises means for receiving address data at the input, storing the address data as the address of the IC, incrementing the address data, and providing the incremented address data at the output. [0051], [0054-0055]

As per claim 5, Massie discloses wherein the address data comprises a binary word.[0063]

As per claim 6, Massie discloses wherein the address data comprises a series of pulses representing an address value. [0050-0051]

As per claim 7, Massie discloses the electronic device further comprising a storage medium in communication with the controller and having stored therein programming instructions for instructing the controller to produce first address data on the output thereof.[0055]

As per claims 8, 9, Massie discloses an electronic device comprising:

- Means for generating first address data at an output of a controller;[0005-0006]

- Means for receiving the first address data at an input of a first IC; [0048-0051]
- Means for storing the first address data in the first IC as an address of the first IC; [0051], [0054-0055], [0063]
- Means for incrementing the first address data in the first IC to produce first incremented address data; and [0048-0051], [0054-0055]
- Means for providing the first incremented address data to a second IC through an output of the first IC. [0048-0051], [0054-0055]

As per claim 10, Massie discloses the method for initializing further comprising:

- Receiving the first incremented address data at an input of a second IC: [0048-0051], [0054-0055]
- Storing the first incremented address data in an address register of the second IC; [0048-0051], [0054-0055]
- Incrementing the first incremented address data in the second IC to produce second incremented address data; and [0048-0051], [0054-0055]
- Providing the second incremented address data at an output of the second IC. [0048-0051], [0054-0055]

As per claim 11, Massie discloses an electronic device comprising:

- A controller; [0005-0006]
 - A plurality of integrated circuits (ICs) addressable by the controller; [0008]
- and

- A shared bus joining the controller and the plurality of integrated circuits;[0048],[0005]
- Wherein the controller is programmed to produce a series of addresses on the shared bus and to produce an enable signal on an output in conjunction with a first address of the series of addresses, [0051], [0054-0055]
- Wherein each of the lcs comprises an input for receiving an enable signal and an output for providing an enable signal in conjunction with a change in address data on the shared bus, and means for storing an address present on the shared bus as an address of the IC in response to receiving an enable signal, and [0051-0052], [0055]
- Wherein the input of a first IC communicates with the output of the controller and the inputs of succeeding lcs communicate with the outputs of preceding lcs in a daisy chain configuration. [0051-54], [0089, claim 7]

As per claim 12, Massie discloses wherein each of said lcs further comprises a first logic circuit for storing an address present on the shared bus as an address of the IC upon receipt of an enable signal.[0051-0052]

As per claim 13, Massie discloses wherein each of said lcs further comprises a second logic circuit for generating an enable signal in conjunction with a change in address data on the shared bus.[0051-0052], [0055]

As per claim 15, Massie discloses wherein said second logic circuit produces an output enable signal upon detecting a first change in address data on the shared bus after receiving an input enable signal. [0063], [0051-0052]

As per claim 16, Massie discloses wherein each of said lcs comprises a processor programmed to initialize a timer upon receipt of an enable signal, and generate an enable signal upon expiration of the timer. [0063], [0051-0052]

As per claim 17, Massie discloses wherein each of said lcs comprises a processor programmed to receive an enable signal at the input, store address data present on the shared bus as the address of the IC in response to the enable signal, detect a change in the address data on the shared bus, and generate an enable signal at the output in response to the change in the address data. [0051-0052]

As per claim 18, Massie discloses wherein each of said lcs comprises:

- Means for receiving an enable signal at the input; and [0051-0052]
- Means for generating an enable signal at the output in conjunction with the change in the address data. [0051-0052]

As per claim 19, Massie discloses the electronic device further comprising a storage medium in communication with the controller and having stored therein programming instructions for instructing the controller to produce a series of addresses on the shared bus and to produce an enable signal on an output in conjunction with a first address of the series of addresses. [0054-0055], [0051]

As per claims 20, 21, Massie discloses an electronic device comprising:

- Means for generating an enable signal at an output of a controller and generating first address data on a shared bus; [0005-0006], [0008]
- Means for receiving the enable signal generated at the output of the controller at an input of a first IC; [0051-0052]
- Means for receiving the first address data at a shared bus input of the first IC; [0048-0051], [0054-0055]
- Means for storing the first address data in an address register of the first IC upon coincidence of the enable signal and the first address data; and [0051], [0054-0055]
- Means for providing an enable signal at an output of the first IC to an input of a second IC in conjunction with a change in address data on the shared bus. [0051-0052]

As per claim 22, Massie discloses a method further comprising:

- Receiving the enable signal provided at the output of the first IC at the input of a second IC; [0048-0051], [0054-0055]
- Storing a second address data present on the shared bus in an address register of the second IC; and [0048-0051], [0054-0055]
- Generating an enable signal at an output of the second IC in conjunction with a change in address data present on the shared bus. [0051-0052]

As per claim 23, wherein generating the enable signal at the output of the first IC comprises initializing a timer upon receipt of the enable signal at the input of the

first IC, and generating the enable signal at the output upon expiration of the timer. [0063]

As per claim 24, Massie discloses wherein the enable signal is generated at the output of the first IC upon detection of a change in address data after receiving an enable signal at the input of the first IC. [0051-0052]

CLAIMS OBJECTION

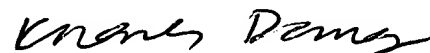
3. Claim 14, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.



Kim Huynh

Nov. 9, 2003

Khanh Dang
Primary Examiner